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EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,939	DAVIS ET AL.	
	Examiner	Art Unit	
	Jason E. Mattis	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-23* is/are allowed.

6)☒ Claim(s) *1-2, 7-19, and 24-26* is/are rejected.

7)☒ Claim(s) *3-6,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 2/17/06. Due to the 37 CFR 1.131 Affidavit, the previous rejections have been withdrawn. Claims 1-28 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 9, 12, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et al. (U.S. Pat. 6775284) in view of McDysan (U.S. Publication US 2004/0208122).

With respect to claim 1, Calvignac et al. discloses a method for packet processing comprising obtaining first information regarding a packet **(See column 10 line 44 to column 11 line 11 and Figure 4 of Calvignac et al. for reference to obtaining information from a packet)**. Calvignac et al. also discloses using the information as an index into a parser memory **(See column 11 lines 12-26 and Figure 4 of Calvignac et al. for reference to using the information to index an ETYPE**

compare memory, a SAP compare memory, and a table 280, which together are a parser memory). Calvignac et al. further discloses retrieving from the parser memory an entry comprising a location in the packet of one or more protocol bits specifying a protocol associated with the packet **(See column 10 line 44 to column 11 line 26 and Figure 4 of Calvignac et al. for reference to retrieving from the ETYPE and SAP compare memories a location of protocol bits associated with the packet)**. Calvignac et al. also discloses obtaining a match engine index **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to using the protocol bits to index the table 280, which outputs a result that is a match engine index on line 276)**. Although Calvignac et al. does disclose using the match engine index as a key to retrieve a match engine entry, comprising an action to take on the packet, from a match engine memory **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to the result on line 276 being used to index an instruction memory 122, which contains entries comprising an action to take on the packet)**, Calvignac et al. does not specifically disclose that both the protocol bits an the match engine index are used as a key to the memory.

With respect to claim 9, Calvignac et al. discloses a method for packet processing in a packet processing system comprising a step for obtaining first information regarding a packet **(See column 10 line 44 to column 11 line 11 and Figure 4 of Calvignac et al. for reference to obtaining information from a packet)**. Calvignac et al. also discloses a step for retrieving an entry corresponding to the first information from a parser memory **(See column 11 lines 12-26 and Figure 4 of**

Calvignac et al. for reference to using the information to index an ETYPE compare memory, a SAP compare memory, and a table 280, which together are a parser memory). Calvignac et al. further discloses a step for retrieving one or more protocol bits identified by the parser memory entry **(See column 10 line 44 to column 11 line 26 and Figure 4 of Calvignac et al. for reference to retrieving from the ETYPE and SAP compare memories a location of protocol bits associated with the packet)**. Although Calvignac et al. does discloses a step for retrieving from a match engine memory a match engine key comprising a match engine index, **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to the result on line 276, which is a match engine index. being used to index an instruction memory 122, which contains entries comprising an action to take on the packet)**, Calvignac et al. does not specifically disclose that both the protocol bits an the match engine index are used as a key to the memory. Calvignac et al. discloses a step for performing the action specified in the retrieved match engine entry **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to performing the action stored in the memory 122)**.

With respect to claim 12, Calvignac et al. discloses a packet processing apparatus comprising a control logic circuit **(See column 10 lines 61 and Figure 4 of Calvignac et al. for reference to a packet processor comprising logic 110)**. Calvignac et al. also discloses a parser memory accessible to the control logic circuit and comprising a plurality of entries each specifying a location in a packet of one or more protocol bits and at least some of which specifying a match engine index **(See**

column 11 lines 12-26 and Figure 4 of Calvignac et al. for reference to an ETYPE compare memory, a SAP compare memory, and a table 280, which together are a parser memory, with the ETYPE compare memory and SAP compare memory having entries specifying to location of protocol bits and the table 280 having entries specifying match engine indexes). Calvignac et al. further discloses a match engine memory accessible to the control logic circuit comprising a plurality of entries each specifying an action to be taken **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to the instruction memory 112, which is a match engine memory, comprising instruction, which are actions, for processing packets)**. Although Calvignac et al. does disclose generating a match engine key using a match engine index and using the match engine key to retrieve from the match engine memory an entry corresponding to the match engine key **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to the result on line 276, which is a match engine index, being used to index an instruction memory 122, which contains entries comprising an action to take on the packet)**, Calvignac et al. does not specifically disclose that both the protocol bits an the match engine index are used as a key to the memory. Calvignac et al. discloses performing the action specified in the retrieved match engine entry **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to performing the action stored in the memory 122)**.

With respect to claim 24, Calvignac et al. discloses a packet processing device **(See column 10 lines 61 and Figure 4 of Calvignac et al. for reference to a packet processor)**. Calvignac et al. discloses a means for retrieving first information about a

received packet **(See column 10 line 44 to column 11 line 11 and Figure 4 of Calvignac et al. for reference to obtaining information from a packet)**. Calvignac et al. also discloses a means for retrieving an entry corresponding to the first information from a parser memory **(See column 11 lines 12-26 and Figure 4 of Calvignac et al. for reference to using the information to index an ETYPE compare memory, a SAP compare memory, and a table 280, which together are a parser memory)**. Calvignac et al. further discloses that the entry comprises one or more protocol bits identified by the parser memory entry **(See column 10 line 44 to column 11 line 26 and Figure 4 of Calvignac et al. for reference to retrieving from the ETYPE and SAP compare memories a location of protocol bits associated with the packet)**. Although Calvignac et al. does discloses a means for retrieving from a match engine memory a match engine key comprising a match engine index, **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to the result on line 276, which is a match engine index. being used to index an instruction memory 122, which contains entries comprising an action to take on the packet)**, Calvignac et al. does not specifically disclose that both the protocol bits an the match engine index are used as a key to the memory. Calvignac et al. discloses a means for performing the action **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to performing the action stored in the memory 122)**.

With respect to claims 1, 9, 12, and 24, McDysan, in the field of communication, discloses using a protocol type as well as other packet header information, to index a table containing instructions regarding the processing of a packet

(See page 4 paragraph 46 of McDysan for reference to using a protocol type along with source and destination addresses of a packet as a lookup key that is used to determine a forwarding port for the packet). Using a protocol type as well as other packet header information, to index a table containing instructions regarding the processing of a packet has the advantage of allowing the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of McDysan, to combine using a protocol type as well as other packet header information, to index a table containing instructions regarding the processing of a packet, as suggested by McDysan, with the system and method of Calvignac et al., with the motivation being to allow the look-up process to be shortened since only the subset of the table that is indexed by the protocol type must be searched for a match.

With respect to claim 2, Calvignac et al. discloses that the match engine index is included in the parser memory **(See column 11 lines 34-54 and Figure 4 of Calvignac et al. for reference to the result on line 276 being included in the table 280)**.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et al. in view of McDysan as applied to claims 1-2, 9, 12, and 24 above, and further in view of Feldmeier et al. (U.S. Pat. 6289414).

With respect to claim 7, the combination of Calvignac et al. and McDysan does not specifically disclose that the match engine memory is a content-addressable memory.

With respect to claim 7, Feldmeier et al., in the field of communications, discloses using a ternary content-addressable memory **(See column 2 line 47 to column 3 line 29 for reference to using a ternary content-addressable memory)**. Using a ternary content-addressable memory has the advantage of being a faster memory, which can help achieve wire speed **(See column 2 line 47 to column 3 line 7 for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Feldmeier et al., to use a ternary content-addressable memory, as suggested by Feldmeier et al., with the system and method of Calvignac et al. and McDysan, with the motivation being to use a faster memory, which can help achieve wire speed.

5. Claims 8, 10-11, 13-19, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et al. in view of McDysan as applied to claims 1-2, 9, 12, and 24 above, and further in view of Paatela et al. (U.S. Publication US 2002/0163935 A1).

With respect to claims 8 and 25, the combination of Calvignac et al. and McDysan. does not disclose that the first information comprises identifying an ATM channel with which a packet is associated.

With respect to claims 8 and 25, Paatela et al., in the field of communications, discloses that obtaining a first information regarding the protocol of a packet comprises identifying a channel with which the packet is associated **(See page 3 paragraph 42 of Paatela et al. for reference to a packet classification being based on the route/flow of the packet, which is a channel that the packet is associated with)**. Paatela et al. also discloses that the channel is an ATM channel **(See page 1 paragraph 9 and page 3 paragraph 42 of Paatela et al. for reference to using ATM packets meaning the flow identified is an ATM flow channel)**. Identifying a channel with which a packet is associated has the advantage of being an easy way to determine the protocol of a packet without having to use any information located in the header of the packet.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to identify a channel with which a packet is associated to determine the protocol of the packet, as suggested by Paatela et al., with the system and method of Calvignac et al. and McDysan, with the motivation being to determine the protocol of a packet without having to use any information located in the header of the packet.

With respect to claim 10, the combination of Calvignac et al. and McDysan does not disclose that the action comprises extracting information relating to another protocol.

With respect to claim 10, Paatela et al., in the field of communications, discloses extracting information relating to another protocol from a packet **(See page 6**

paragraph 63 of Paatela et al. for reference to extracting information from a different MPLS protocol header and moving the different header to the top of the MPLS protocol stack of the packet). Extracting information relating to another protocol from a packet has the advantage of allowing a packet to be processed at multiple protocol layers using the same device.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to extract information relating to another protocol from a packet, as suggested by Paatela et al., with the system and method of Calvignac et al. and McDysan, with the motivation being to allow a packet to be processed at multiple protocol layers using the same device.

With respect to claims 11 and 26, Calvignac et al. discloses that the action consists of forwarding the packet **(See column 3 line 66 to column 4 line 14 for reference to the invention being implement in a router meaning there must be instruction to route, or forward packets)**.

With respect to claims 13-16, the combination of Calvignac et al. and McDysan does not disclose that the control logic circuit comprises an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contains an interface to the external memory.

With respect to claims 13-16, Paatela et al., in the field of communications, discloses control logic circuit comprising an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contain an interface to the external memory **(See page 5 paragraphs 57-58 and**

Figures 5-6 of Paatela et al. for reference to the components of the control logic circuit being included on a single integrated circuit with the memories and buffers optionally being either incorporated into the common chip or external to the common chip, with the common chip including interfaces to an external memory). Using a control logic circuit comprising an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contain an interface to the external memory has the advantage of allowing the memories of the system to be flexible in size and type such that they do not have to be located on in the same device as the control circuit.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Paatela et al., to use a control logic circuit comprising an integrated circuit with memories that are either integrated with the control logic circuit or external to the control logic circuit that contain an interface to the external memory, as suggested by Paatela et al., with the system and method of Calvignac et al. and McDysan, with the motivation being to allow the memories of the system to be flexible in size and type such that they do not have to be located on in the same device as the control circuit.

With respect to claims 17-18, although the combination of Calvignac et al., McDysan, and Paatela et al. does not specifically disclose that the parser memory and match engine memory comprise 512 or fewer entries, the size of the memories used in the packet processing apparatus are an obvious design choice that a user would make at the time of designing the apparatus. Choosing the exact size of the memory has the

advantage of allowing the memory and memory access keys to be customized to the desired size of a user.

It would have been obvious for one of ordinary skill in the art at the time of the invention to choose the size of the memories to fit the needs of a user of the apparatus with the motivation being to allow memory and memory access keys to be customized to the desired size of a user.

With respect to claim 19, Calvignac et al. discloses that the control logic circuit comprises a pipelined architecture **(See Figure 4 of Krishnan et al. for reference to the processor having a pipelined architecture)**.

Allowable Subject Matter

6. Claims 20-23 are allowed.

7. Claims 3-6 and 27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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